CLAIMS

Subt C' What is claimed is:

1. A method of forming an isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

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2. The method of claim 1, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

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3. The method of claim 1, wherein selectively etching said portion of said ~~buffer film layer includes horizontal and vertical etching of said buffer film layer~~.

Sub B'

4. The method of claim 3, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

5. The method of claim 1, further including annealing said isolation material layer.

6. An isolation structure for a semiconductor device formed by the method comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

7. The isolation structure of claim 6, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

8. The isolation structure of claim 6, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

9. The isolation structure of claim 8, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

10. The isolation structure of claim 6, formed by a method further comprising annealing said isolation material layer.

11. A method of forming a capped shallow trench isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench sidewalls and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

12. The method of claim 11, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

13. The method of claim 11, wherein selectively etching said portion of said ~~buffer film layer includes horizontal and vertical etching of said buffer film layer.~~

14. The method of claim 13, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

15. The method of claim 11, further including annealing said isolation material layer.

16. The method of claim 11, wherein said capped shallow trench isolation structure includes ledges which extend a predetermined distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

17. The method of claim 16, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.

18. A capped shallow trench isolation structure formed by the method comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench sidewalls and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

19. The capped shallow trench isolation structure of claim 18, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

20. The capped shallow trench isolation structure of claim 18, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

21. The capped shallow trench isolation structure of claim 20, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

22. The capped shallow trench isolation structure of claim 18, formed by a method comprising annealing said isolation material layer.

23. The capped shallow trench isolation structure of claim 18, wherein said capped shallow trench isolation structure includes ledges which extend a predetermined distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

24. The capped shallow trench isolation structure of claim 23, wherein said ledges extend over said semiconductor substrate between about 50 and 150Å.

25. A method of forming an isolation structure on semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, wherein an oxide layer is formed on exposed portions of said semiconductor substrate within said trench, comprising:

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

26. The method of claim 25, wherein selectively etching said portion of said ~~buffer film layer includes horizontal and vertical etching of said buffer film layer~~.

27. The method of claim 26, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

28. The method of claim 25, further including annealing said isolation material layer.

29. An isolation structure for a semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, wherein an oxide layer is formed on exposed portions of said semiconductor substrate within said trench, formed by the method comprising:

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer to fill said trench; removing a portion of said isolation material layer above said buffer film layer; and removing said buffer film layer.

30. The isolation structure of claim 29, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

31. The isolation structure of claim 30, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

32. The isolation structure of claim 29, formed by a method further comprising annealing said isolation material layer.

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33. A method of forming a capped shallow trench isolation structure for a semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, wherein an oxide layer is formed on exposed portions of said semiconductor substrate within said trench, comprising:

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

34. The method of claim 33, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

35. The method of claim 34, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

36. The method of claim 33, further including annealing said isolation material layer.

37. The method of claim 33, wherein said capped shallow trench isolation structure includes ledges which extend a predetermined distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

38. The method of claim 37, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.

39. A capped shallow trench isolation structure for a semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, wherein an oxide layer is formed on exposed portions of said semiconductor substrate within said trench, formed by the method comprising:

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

40. The capped shallow trench isolation structure of claim 39, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

41. The capped shallow trench isolation structure of claim 40, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

42. The capped shallow trench isolation structure of claim 39, formed by a method comprising annealing said isolation material layer.

43. The capped shallow trench isolation structure of claim 39, wherein said capped shallow trench isolation structure includes ledges which extend a predetermined distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

44. The capped shallow trench isolation structure of claim 43, wherein said ledges extend over said semiconductor substrate between about 50 and 150Å.

45. A shallow trench isolation structure, having integral ledges which extend a predetermined distance from a trench formed in a semiconductor device layered structure including a semiconductor substrate, a dielectric layer, and a buffer film

layer, said trench extending through said buffer film layer, said dielectric layer, and into said semiconductor substrate, formed by the method comprising:

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer to expose opposing trench edges at an intersection of said trench and an upper surface of said semiconductor substrate;

applying a layer of isolation material over said buffer film layer to fill said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

46. The shallow trench isolation structure of claim 45, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

47. The shallow trench isolation structure of claim 45, wherein selectively etching said portion of said buffer film layer includes horizontal and vertical etching of said buffer film layer.

48. The shallow trench isolation structure of claim 47, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a predetermined distance from said trench.

49. The shallow trench isolation structure of claim 45, formed by a method comprising annealing said isolation material layer.

50. The shallow trench isolation structure of claim 45, wherein said ledges extend over said semiconductor substrate between about 50 and 150Å.

51. A capped shallow trench isolation structure comprising a homogenous isolation material disposed within a trench in a semiconductor substrate, wherein said homogenous isolation material includes ledges which extend a predetermined distance over an upper surface of said semiconductor substrate from said trench.

52. The capped shallow trench isolation structure of claim 51, wherein said ledges extend over said semiconductor substrate between about 50 and 150Å from said trench.